

**REMARKS**

Claims 1-36 were previously pending in this application. By this amendment, Applicant is canceling claims 11-13, 21 and 22 without prejudice or disclaimer. Claims 3, 10, 14, 16, 17, 18, 20, 23, 25, 29, 30 and 34 have been amended. No new claims have been added. As a result claims 1-10, 14-21 and 23-36 are pending for examination with claims 1, 10, 16, 20, 25, 29, 30 and 34 being independent claims. No new matter has been added.

**Specification**

The Examiner objected to the title of the invention as not descriptive. The title has been replaced hereby with a title whose language tracks the language of the claims in this case. The new title is therefore appropriate. Withdrawal of this objection is respectfully requested.

**Drawings**

The Examiner objected to the drawings on two grounds. Figures 1-3 depict that which is known in the art, but did not include a legend such as "Prior Art," while the drawings as a whole fail to include all the reference designations referred to in the written description. Corrected drawing sheets are provided herewith, overcoming this objection, except where the objection is traversed as noted below. Withdrawal of this objection is respectfully requested.

Figures 1-3 each now bear the legend "Prior Art" as required.

Figure 2 has been amended to include a reference designation **200** identifying the circuit, generally, as the reference designation has been used in the written description.

As for the objection concerning  $V_{DD}$ , this Applicant notes that  $V_{DD}$  appears in various locations of Figures 4, 5, 6 and 8. Based on those appearances, as well as the convention, known in the art, that the term  $V_{DD}$  signifies the drain supply voltage in CMOS circuits, the use of the term in the drawings and the written description is both clear and complete. If the Examiner is of the opinion that  $V_{DD}$  should appear at some specific location where it does not presently appear in one of the Figures, the Examiner is invited to point out that location to the Applicant. Absent such an indication, this portion of the objection is respectfully traversed.

### Claim Objections

The Examiner objected to claim 25 for informality. The phrase “the differential amplifier circuit” did not have antecedent basis, although it was clearly intended to reference the “auto-zero amplifier” introduced earlier in the claim. Claim 25 has been rewritten to correct the informality by replacing each occurrence of “the differential amplifier” with “the auto-zero amplifier.” Withdrawal of this objection is respectfully requested.

### Rejections Under 35 U.S.C. §102

Claims 10, 12, 19 and 29 have been rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,570,617 B2 to Fossum et al. (hereinafter *Fossum*). Claims 10 and 29 have been amended, overcoming this rejection as to those claims, as explained below. Claim 19 overcomes the rejection for the same reasons as claim 10, from which claim 19 depends. Claim 12 has been cancelled, rendering the rejection moot as to claim 12.

Claim 10 has been amended to combine the subject matter of claims 10, 11 and 13. Claim 10 thus now recites the subject matter of claim 13 in independent form, including the base claim (10) and intervening claim (11) from which claim 13 depended. Claim 13 was not subject to the instant rejection. Therefore claim 10 is now no longer subject to this rejection.

Claim 29 has been amended to include the elements of “a differential amplifier circuit” and “coupling the sample and hold circuit to the differential amplifier within a feedback loop.” This is similar to the distinguishing language from claims 11 and 13, now incorporated in amended claim 10. Therefore, claim 29 is now no longer subject to this rejection.

Accordingly, withdrawal of this rejection is respectfully requested.

Claims 20-22, 26-28, 30 and 36 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,633,029 B2 to Zarnowski et al. (hereinafter *Zarnowski*). Claim 20 has been amended to combine the subject matter of claims 20, 21 and 22. The rejection of amended claim 20 (original claim 22) is traversed, as explained below. Claims 26-28 all depend from claim 20, and are therefore allowable for at least the same reasons as described in connection with claim 20. Claim 30 has been amended overcoming this rejection, as explained below, and claim 36 has been cancelled, rendering the rejection moot as to that claim.

*Zarnowski* discloses, for example, in Fig. 2, an image sensor circuit including a photogate or photodiode 10, a differential amplifier 30 and a correlated double sampler 34. The differential

amplifier 30 of *Zarnowski* includes a differential transistor pair 15 and 24, and is connected in a feedback configuration by signal 32 as a unity-gain follower. However, *Zarnowski* does not disclose a sample and hold circuit or a clamp circuit. It is asserted that all circuits for performing correlated double sampling (CDS) inherently include sample and hold elements and that the CDS block 34 includes a sample and hold circuit within a feedback loop 32, but this element is not shown in *Zarnowski*. The only element shown in Fig. 2 of *Zarnowski* that can include the sample and hold circuit feature is the CDS block 34, and the CDS block 34 is outside of feedback connection 32. Thus, to the extent that this circuit may be present in the circuit disclosed, it must be contained in the CDS block 34, and outside of feedback loop 32.

While it is known and natural in the art to provide an amplifier circuit with feedback, in order to improve the performance of the amplifier by reducing noise and other non-linear effects, there is no teaching or suggestion in these references to include the sample and hold circuits within the feedback loop. Indeed, *Zarnowski* could have shown or suggested just such an arrangement, but did not so much as hint at the claimed topology. Instead, *Zarnowski* simply condenses all the elements required to perform CDS into a single block labeled “CDS,” block 34 as explained above, while the feedback loop 32 encloses only the differential amplifier stage 30. Thus, there is no disclosure, teaching or suggestion in this reference to make the claimed invention.

Claim 20 recites a feedback loop that encloses both the amplifier circuit and the sample and hold circuits. That is, the “sampling circuitry includes a sample and hold circuit coupled within said feedback path.” In contrast, *Zarnowski* discloses applying feedback only to the amplifier circuit, leaving the sample and hold function outside of the feedback loop. Thus, *Zarnowski* fails to disclose all of the elements of the claimed invention.

Accordingly, withdrawal of this rejection with respect to claim 20 is respectfully requested.

As amended, claim 30 now recites

a feedback loop amplifier circuit having said photo sensing node voltage as one input, and a sample and hold circuit having an output coupled to a second input of the feedback loop amplifier circuit, to form a feedback loop; a clamping circuit coupled to the output from the sample and hold circuit and which produces an output signal representing a double correlated sample voltage difference at said photo sensing node.

Thus, claim 30 also encloses within the feedback path both the feedback loop amplifier and the sample and hold circuit. As noted above, *Zarnowski* discloses applying feedback only to the amplifier circuit, does not disclose a sample and hold circuit, and therefore does not disclose or suggest any sample and hold circuit within the feedback loop. Thus, *Zarnowski* fails to disclose all of the elements of the claimed invention.

Accordingly, withdrawal of this rejection is respectfully requested.

#### Rejections Under 35 U.S.C. §103

Claims 1-9 have been rejected under 35 U.S.C. §103(a) as being unpatentable over *Fossum* in view of U.S. Patent No. 6,438,276 B1 to Dhuse et al. (hereinafter *Dhuse*). As admitted by the Office Action, *Fossum* does not disclose wherein the correlated double sampling comprises following the photo sensing node voltage from a first time instant occurring after completion of a said integration phase and before instigation of a subsequent said reset phase, to a second time instant occurring after completion of said subsequent reset phase. However, the Office Action asserts that *Dhuse* discloses correlated double sampling comprising following the photo sensing node voltage from a first time instant occurring after completion of a said integration phase and before instigation of a subsequent said reset phase, to a second time instant occurring after completion of said subsequent reset phase. This rejection is traversed, as follows.

*Fossum* discloses generally a pixel sensor circuit, for example, in Figs. 5A and 5B, including a photogate, an amplifier, sample and hold, and clamp circuitry. *Dhuse* discloses correlated double sampling (CDS) performed in a conventional sequence of first measuring the reset voltage and then measuring the voltage after sample integration.

As explained by the Applicant, beginning at page 25, line 9 of the written description, the inventive CDS sequence is advantageous because it reduces the amount of feedthrough noise present on the output signal. One component of the inventive method, recited in claim 1 and emphasized in the description pointed out, is the order in which the measurements of the sample and hold outputs are made. Making those measurements in the claimed order provides the advantage of improved feedthrough noise performance, as compared to the prior art. This unexpected result was recognized, described and claimed by the Applicant.

In particular, claim 1 calls for a method including correlated double sampling performed by measuring the sampled voltage *after* a first pixel integration ( $V_1^1$ ) and then measuring the

sampled voltage again after performing the reset that precedes the *next* pixel integration ( $V_R^2$ ). The difference computed based on this sample sequence is  $V_I^1 - V_R^2$ .

In contrast, contrary to the assertion of the Office Action, *Dhuse* teaches a conventional sequence comprising measuring the reset voltage that *precedes* a pixel integration ( $V_R^1$ ) followed by measuring the voltage *after* the pixel integration ( $V_I^1$ ). See Fig. 6, step 606 and the description of column 7, line 48-column 8, line 3, especially the last sentence. Thus, *Dhuse* teaches computing a difference of  $V_R^1 - V_I^1$ .

It is clear from the foregoing discussion that the claimed method differs from the proposed combination. The difference produced by the invention claimed in claim 1, which claims  $V_I^1 - V_R^2$ , differs both in value and effect from that produced by *Dhuse*, either alone or in combination with *Fossum*, which is  $V_R^1 - V_I^1$ . The prior workers in this art, as suggested by the assorted combination, employ as the only order for measuring the sample and hold output discussed or suggested in the references, the natural order for the measurement, which is to measure the reset voltage that *precedes* a pixel integration ( $V_R^1$ ) followed by measuring the voltage *after* the pixel integration ( $V_I^1$ ). Not only do the two different methods produce different results, on their face, but the method of the combination does not suggest the claimed method. The claimed method provides novel advantages not realized or understood by prior workers in this art.

Accordingly, withdrawal of this rejection is respectfully requested.

Claims 11, 13 and 17 have been rejected under 35 U.S.C. §103(a) as being unpatentable over *Fossum* in view of *Zarnowski*. Claims 11 and 13 have been cancelled, rendering this rejection moot as to claims 11 and 13. The rejection is traversed as to 17 which has been amended to depend from claim 10.

Claim 17 depends from claim 10 which has been amended to include the recitation of claim 13, and recites a feedback loop that encloses both the amplifier circuit and the sample and hold circuits. As has been pointed out, herein, *Fossum* does not employ a feedback loop at all, while *Zarnowski* teaches applying feedback only to the amplifier circuit, leaving the sample and hold function outside of the feedback loop.

As has been explained above, there is no teaching or suggestion to provide feedback that includes within the feedback loop the sample and hold circuits. Thus, there is no teaching or suggestion in this combination of references to make the claimed invention.

Accordingly, withdrawal of this rejection is respectfully requested.

Claims 14 and 18 have been rejected under 35 U.S.C. §103(a) as being unpatentable over *Fossum* in view of *Zarnowski*, and further in view of U.S. Patent No. 6,421,085 B1 to Xu (hereinafter *Xu*). This rejection is traversed as follows.

Claims 14 (dependency as amended) and 18 depend from claim 10, which now recites a feedback loop that encloses both the amplifier circuit and the sample and hold circuits. As discussed above, the combination of *Fossum* with *Zarnowski* teaches applying feedback only to the amplifier circuit, leaving the sample and hold function outside of the feedback loop. *Xu* does not cure the infirmities of the asserted combination of *Fossum* and *Zarnowski*, and does not add any teaching in this regard. *Xu* discloses and teaches only a correlated double sampling unit for a CMOS imager, without a feedback connection as recited in claim 10. Therefore, these claims are unobvious for at least the same reasons as given above with respect to claim 10.

Accordingly, withdrawal of this rejection is respectfully requested.

Claim 15 has been rejected under 35 U.S.C. §103(a) as being unpatentable over *Fossum* in view of *Zarnowski* in view of *Xu* and further in view of U.S. Patent No. 6,137,535 to Meyers (hereinafter *Meyers*). This rejection is traversed as follows.

Claim 15 depends (*inter alia*) from claim 10. Like *Xu*, discussed above, *Meyers* also does not cure the infirmities of the asserted combination of *Fossum* and *Zarnowski*, and does not add to the combination any teaching or suggestion of the feedback arrangement of claim 10. Like *Xu*, *Meyers* discloses and teaches a correlated double sampling unit without a feedback connection as recited in claim 10. Therefore, for at least the same reasons as discussed above with respect to claim 10, claim 15 is non-obvious in view of this combination.

Moreover, *Meyers* does not teach or suggest the topology recited in claim 15 for the sampling circuit and the clamping circuit because the elements relied upon by the Examiner do not correspond with the elements of the claim or the asserted combination of *Fossum* and *Zarnowski*, and no other elements taught by *Meyers* correspond with the elements of the claim or the asserted combination of *Fossum* and *Zarnowski*. Therefore, the suggestions drawn by the Examiner from the references for adding *Meyers* to the combination simply cannot exist.

Referring to Figs. 6, 7 and 8, the Examiner has identified amplifiers 42 and 44 as sample and hold circuits and has identified amplifier 46 and the associated capacitor and FET as a clamping circuit. The Applicant respectfully disagrees.

*Meyers* describes Fig. 7, in relevant portion, at column 11, lines 38-63. As described therein, amplifiers 42 and 44 are matched, current amplifiers with opposite gains. They are used in a configuration referred to as dual slope (referring to the opposite gains) CDS, in which one amplifier operates while the shutter of the system is open and the other operates while the shutter of the system is closed. Thus, neither amplifier actually “samples” or “holds” any current or voltage value, but rather current is steered through one or the other, alternately driving current into and sinking current out of the subsequent integration stage in a continuous time sequence. Amplifier 46 and the associated capacitor integrate the current to produce the correlated double sample. The FET is simply the reset switch to clear all charge from the capacitor. The correlated double sample is thus produced by the integration performed by amplifier 46, whereupon it is transferred to an analog-to-digital converter 56. Thus, *Meyers* does not have the sample and hold and clamp circuits of the claim.

Accordingly, withdrawal of this rejection is respectfully requested.

Claims 23, 31 and 35 have been rejected under 35 U.S.C. §103(a) as being unpatentable over *Fossum* in view of *Zarnowski* in view of *Xu*. Claim 23 depends from claim 20, and is allowable for at least the same reasons as claim 20. Claims 31 and 35 depend from claim 30 and are allowable for at least the same reasons as claim 30. In particular, as has been shown above, *Zarnowski* does not disclose the inventions of claims 20 and 30. Reading *Fossum* in view of *Zarnowski* and *Xu*, the combination does not teach or suggest the claimed inventions because the asserted combination does not teach or suggest the feedback path recited in claims 20 and 30. None of these references teach the claimed topology, either alone or in combination. Therefore, these claims, which are dependent from claims 20 and 30, are also patentable over the asserted combination.

Accordingly, withdrawal of this rejection is respectfully requested.

Claim 24 has been rejected under 35 U.S.C. §103(a) as being unpatentable over *Zarnowski* in view of *Xu* and further in view of U.S. Patent No. 6,753,912 B1 to Wayne (hereinafter *Wayne*). Claim 24 depends from claim 20, and is allowable for at least the same reasons as claim 20. Namely, as discussed previously, *Zarnowski* does not disclose the invention of claim 20. The asserted combination of *Zarnowski*, *Xu* and *Wayne* fail to teach or suggest the feedback path of claim 20 because none of these references teach the claimed topology, either

alone or in combination. Therefore, claim 24, dependent from claim 20, is also patentable over the asserted combination.

Accordingly, withdrawal of this rejection is respectfully requested.

Claim 32 has been rejected under 35 U.S.C. §103(a) as being unpatentable over *Zarnowski* in view of *Wayne*. Claim 32 depends from claim 30, and is allowable for at least the same reasons as claim 30. The invention claimed by claim 30 is not disclosed by *Zarnowski*, as discussed above. Combining *Zarnowski* with *Wayne* fails to teach or suggest the feedback path of claim 30 because neither reference teaches the claimed topology, either alone or in combination. Therefore, claim 32, dependent from claim 30, is also patentable over the combination.

Accordingly, withdrawal of this rejection is respectfully requested.

Claim 33 has been rejected under 35 U.S.C. §103(a) as being unpatentable over *Zarnowski* in view of *Wayne* and further in view of *Meyers*. Claim 33 depends from claim 32, and thus from claim 30, and is allowable for at least the same reasons as claim 32 (and thus, also for the same reasons as claim 30). The application of *Zarnowski* to claim 30 has been discussed above. As with the combinations discussed above, combining *Zarnowski* with *Wayne* and *Meyers* still does not teach or suggest the invention of claim 30. None of these references, either alone or in combination, teach or suggest the topology of the feedback path claimed.

Accordingly, withdrawal of this rejection is respectfully requested.

#### Allowable Subject Matter

The Applicant thanks the Examiner for the indication of allowable subject matter in claims 16, 25 and 34. Claims 16, 25 and 34 have been rewritten in independent form, including all of the subject matter recited in the base and intervening claims from which they depend.

#### Corrections

Claims 3 and 18 have been amended for reasons unrelated to the Examiner's rejection. A typographical omission has been corrected in claim 3. The word "to" has been inserted in the second line of the claim. Claim 18 has been amended for greater clarity by now referring to the antecedent "feedback loop" where arrangement gives the amplifier its gain in the claimed topology.




**CONCLUSION**

In view of the foregoing amendments and remarks, reconsideration is respectfully requested. This application should now be in condition for allowance; a notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

Applicant hereby requests a one-month extension of time. If the fee occasioned by this response, including an extension fee covered by an enclosed check is insufficient, please charge any deficiency to Deposit Account No. 50/2762.

Respectfully submitted,  
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**Amendments to the Drawings**

Please replace Figures 1 – 3, contained in drawing sheets 1/8 – 3/8 with the figures in the attached replacement sheets.